ABSTRACT OF THE DISCLOSURE

A memory device with multiple bits per cell. The memory device includes a side electrode; a doped semiconductor region disposed laterally in contact with a sidewall of the side electrode, such that the doped semiconductor region forms a diode, or the junction between the side electrode and the doped semiconductor region forms a diode; a layer of phase-changing material disposed laterally in contact with a sidewall of the doped semiconductor region, such that the doped semiconductor region is disposed between the layer of phase-changing material and the side electrode; and an upper electrode disposed on the layer of phase-changing material. Many storage regions can be stacked vertically, and multiple bits can be stored in one cell. Also, the contact area is reduced to a minimum dimension below the photolithographic limit.